REMARKS

The Office Action mailed August 18, 2004, has been received and reviewed. Claims 1 through 25 are currently pending in the application. Claims 1 through 25 stand rejected. Applicant has amended claims 1, 6, 8, 17, 21 and 23, and respectfully request reconsideration of the application as amended herein.

Preliminary Amendment

Applicant's undersigned attorney notes the filing herein of a Preliminary Amendment on February 13, 2004, which filing was not acknowledged in the outstanding Office Action. Should the Preliminary Amendment have failed for some reason to have been entered in the Office file, Applicant's undersigned attorney will be happy to have a true copy thereof hand-delivered to the Examiner.

Double Patenting Rejection Based on U.S. Patent No. 6,732,223

Claims 1 through 4, 6, 8, 10 through 17, 19 and 25 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 through 3, 5, 7 through 11, 14, 15 and 19 of U.S. Patent No. 6,732,223.

Claims 5 and 7 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 4 (respectively) of U.S. Patent No. 6,732,223 in view of Rust et al. (U.S. Patent No. 5,699,530).

Claims 9, 18, 20 through 22 and 24 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 7 or 8, 11, or 15 of U.S. Patent No. 6,732,223 in view of Hang (U.S. Patent No. 5,487,049).

In order to avoid further expenses and time delay, Applicant elects to expedite the prosecution of the present application by filing Terminal Disclaimers to obviate the double patenting rejections in compliance with 37 CFR §1.321 (b) and (c). Applicant's filing of the Terminal Disclaimers should not be construed as acquiescence of the Examiner's double patenting or obviousness-type double patenting rejections. Attached are the Terminal Disclaimers and accompanying fees.

35 U.S.C. § 112 Claim Rejections

Claims 1 through 5, and 13 through 24 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regard as the invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

Specifically, the Office Action states:

> As per claim 1, 13, 17, and 23, Applicant sets forth in the claims that the "data corresponding to the memory command arrives at the DRAM", implying that the data does not travel through the FIFO. Applicant also set forth "simultaneous reading and writing of the at least one of data and commands from the FIFO", indicating that the data travels through the FIFO. It is not clear from the amended claim language whether the data travels through the FIFO or not. For purposes of applying the prior art, the Examiner will assume that the data travels through the FIFO. (Office Action, p. 6).

Applicants respectfully disagree with the Examiner's characterization of the claim language.

Claim 1 and Claim 13

Applicants assert that claims 1 and 13 as amended and previously presented are drawn to more particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, Applicants claim "A . . . DRAM, comprising:", "a FIFO associated with the control logic, the FIFO configured for temporarily storing at least one memory command within the DRAM" and "a FIFO associated with the control logic, . . . the control logic further configured for simultaneous reading and writing from the FIFO." (Amended independent claim 1 with claim 13 being similarly drawn). Specifically, the DRAM of claims 1 and 13, include "at least one memory bank . . ., control logic associate with the at least one memory bank . . ., and a FIFO associated with the control logic . . .." Therefore, Applicants' respectfully request that the rejection be withdrawn.

Claim 17

Applicants have amended claim 17 to more particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, Applicants claim a method of storing data in a DRAM which includes a FIFO configured for temporarily storing a memory

bank address command". It is possible, as configured, for a form of data to arrive at an exterior interface to the DRAM but not be stored within the temporary storage of the FIFO, however, Applicants claim as amended removes any ambiguity with respect to the FIFO being configured to temporarily store a memory bank address command therein. Therefore, if a command is stored even temporarily within the FIFO it then, in fact, "passes through the FIFO." Accordingly, Applicants' respectfully request that the rejection be withdrawn.

Claim 23

Applicants assert that claim 23 as presently presented is drawn to more particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, Applicants claim a method of buffering a data stream . . ., the method comprising: providing a FIFO buffer system having . . . a series of FIFO buffers . . . configured for temporarily storing the memory band address command while retrieving the data corresponding to the memory bank address command . . .."

Therefore, if a memory band address command is stored even temporarily within the FIFO it then, in fact, "passes through the FIFO." Accordingly, Applicants' respectfully request that the rejection be withdrawn.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,487,049 to Hang

Claims 1 through 4, 6, and 17 through 25 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Hang (U.S. Patent No. 5,487,049). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicants submit that the Hang reference does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of independent claims 1, 6, 17, 23, 25 and claims 2-5, 18-22 and 24 depending therefrom because the Hang reference does not describe, either expressly or inherently, the identical inventions in as complete detail as are contained in the claims. More specifically, Applicants submit that the Hang reference does not describe, either expressly or inherently, the elements of the claimed inventions of independent claims 1, 6, 17, 23 and 25.

The Hang reference discloses:

> a FIFO interface between a system bus and a DRAM that transfers data to the DRAM utilizing the high speed page mode [wherein] words transferred having the same row address are accumulated in a store and then transferred to the DRAM utilizing the page mode to reduce the transfer time.
>
> According to another aspect of the invention, the words stored in FIFO are transferred to the DRAM when the row address of a next word to be stored changes so that the page mode transfer can be utilized. (Col. 1, lines 39-48).

In essence, the Hang reference discloses using a FIFO in conjunction with a memory device for buffering ***data that is to be transferred to memory once the command configures the control circuitry in a page mode configuration.*** Generally, Hang allows the memory command to ***configure the memory*** (in contrast to the memory command being stored in the FIFO) to operate in page mode and then ***buffer-up*** or burst-out ***memory data*** rather than buffering memory commands as claimed by the Applicants. In contrast and generally opposite, Applicants' inventions as respectively claimed in the independent claims are drawn to, for example:

Independent Claim 1

> a . . . FIFO ***configured for*** temporarily ***storing at least one memory command*** until at least one of the data corresponding to the memory command arrives at the DRAM . . .

Independent Claim 6

> a FIFO ***configured for*** temporarily ***storing at least one memory command until at least one data*** corresponding to the memory command arrives at the DRAM;

Independent Claim 17

a FIFO . . . ***configured for temporarily storing a memory bank address command*** until data corresponding to the memory bank address command arrives at the DRAM,

Independent Claim 23

providing a FIFO buffer system having . . . a FIFO including . . . FIFO buffers ***configured for temporarily storing the memory bank address command*** while retrieving the data corresponding to the memory bank address command;

Independent Claim 25

temporarily ***storing in a FIFO a first of the at least one memory bank address command***, . . . temporarily storing in the FIFO a second of the at least one memory bank address command; . . . storing in the FIFO the data corresponding to the first of the at least one memory bank address command . . .; and storing in the FIFO the data corresponding to the second of the at least one memory bank address command.

Therefore, independent claims 1, 6, 17, 23, 25 and claims 2-5, 18-22 and 24 depending therefrom are not anticipate by the Hang reference under 35 U.S.C. § 102. Therefore, the Hang reference cannot anticipate Applicants' invention as claimed. Accordingly, Applicants' respectfully request that the rejection be withdrawn as such claims are allowable over the cited prior art.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in view of U.S. Patent No. 5,699,530 to Rust et al.

Claims 5 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Rust et al. (U.S. Patent No. 5,699,530). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or**

> **references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 5 and 7 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must each or suggest all the claim limitations.

Regarding claim 5 depending at least indirectly from independent claim 1, Hang and Rust, either individually or in any proper combination, do not teach, suggest or motivate the claim limitations of

> a . . . FIFO configured ***for*** temporarily ***storing at least one memory command*** until at least one of the data corresponding to the at least one memory command arrives at the DRAM . . ..

Applicants herein sustain the above-arguments for the lack of teaching or suggestion in Hang for a FIFO for storing commands while awaiting corresponding data which is in direct juxtaposition of the Hang teachings. The Office Action cited Rust for teachings of "linear shift registers" which does not augment Hang's deficiencies regarding a command-storing FIFO, as claimed by Applicants. Therefore, Applicants respectfully request that the rejection of claim 5 be withdrawn.

Regarding claim 7, Hang and Rust, either individually or in any proper combination, do not teach, suggest or motivate the claim limitations of

> a . . . FIFO configured ***for*** temporarily ***storing at least one memory command*** until at least one data corresponding to the at least one memory command arrives at the DRAM . . ..

Applicants herein sustain the above-arguments for the lack of teaching or suggestion in Hang for a FIFO for storing commands while awaiting corresponding data which is in direct juxtaposition of the Hang teachings. The Office Action cited Rust for teachings of "linear shift registers" which does not augment Hang's deficiencies regarding a command-storing FIFO, as claimed by

Applicants. Therefore, Applicants respectfully request that the rejection of claim 7 be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in view of U.S. Patent No. 5,289,584 to Thome et al.

Claims 8 through 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Thome et al. (U.S. Patent No. 5,289,584). Applicant respectfully traverses this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 8-10 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must each or suggest all the claim limitations.

Regarding independent claim 8 and claims 9 and 10 depending therefrom, Hang and Thome, either individually or in any proper combination, do not teach, suggest or motivate the claim limitations of

> at least one FIFO ***configured for temporarily storing at least one of the instructions until at least one of the data corresponding to the at least one of the instructions arrives at the memory device*** . . ..

Applicants herein sustain the above-arguments for the lack of teaching or suggestion in Hang for a FIFO for storing commands while awaiting corresponding data which is in direct juxtaposition of the Hang teachings. The Office Action cited Thome for teachings of "a system including a

page mode DRAM and a FIFO 114 or 116 (figure 2), which includes a CPU 30, keyboard 80 ("input device"), monitor 64 ("output device") and a hard disk 98 ("storage device")" which does not augment Hang's deficiencies regarding a command-storing FIFO, as claimed by Applicants. Therefore, Applicants respectfully request that the rejection of claim 8, and claims 9 and 10 depending therefrom, be withdrawn.

Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in view of U.S. Patent No. 5,426,612 to Ichige et al.

Claims 11 and 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Ichige et al. (U.S. Patent No. 5,426,612). Applicant respectfully traverses this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 11 and 12 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must each or suggest all the claim limitations.

Regarding independent claim 11 and claim 12 depending therefrom, Hang and Ichige, the Office Action states:

> As per claims 11 and 12, Hang teaches the invention as set forth above for claim 6. However, Hang does not teach that the system is embodied on a semiconductor substrate (semiconductor wafer). Ichige et al. teaches that it was known in the art at the time the invention was made to incorporate a FIFO with associate pointer logic on a single semiconductor substrate/wafer. (Office Action pp. 11-12).

Regarding the Office Action's characterization of Hang's teachings "as set forth above for claim 6", the Office Action states:

> As per claim 6, Hang teaches a FIFO system 10 including a FIFO data buffer 30 and address buffer 34, a write counter 22, and a read counter 26. See figure 1. Hang teaches that the read counter 26 is incremented upon a particular assertion of DRAM REQ. See column 4, lines 24-26. Therefore, prior to the read operation, the read counter register is configured to maintain the previous read counter setting. (Office Action p. 8).

Regarding claim 11, Hang teaches or suggests a page mode-directed FIFO, as herein described by the Office Action. However, Hang does not appear to teach or suggest each and every claim limitation of claim 11 as set forth herein. Specifically, Hang does not teach or suggest:

> 11. A semiconductor substrate including a FIFO buffer, comprising:
> at least one FIFO;
> at least one write counter associated with the at least one FIFO; and
> at least one read counter associated with the at least one FIFO, the at least one read counter comprising at least one pointer register configured to maintain a previous read counter setting of the at least one read counter.

While it is a given fact that ***before*** something transitions form a first state to a second state, it does in fact indicate the first state, nothing within Hang teaches or suggests or appears to be in any need of a "at least one pointer register configured to maintain a previous read counter setting of the at least one read counter", as claimed by Applicants.

As stated, the Office Action cited Ichige for it teachings relating to "a FIFO with associated pointer logic on a single semiconductor substrate/wafer" which does not augment the teachings of Hang in such a manner as to render obvious Applicants' invention as claimed. Therefore, Applicants respectfully request the rejection of claim 11 and claim 12 depending therefrom be withdrawn.

<u>Obviousness Rejection Based on U.S. Patent No. 5,487,049 to Hang in view of U.S. Patent No. 6,329,997 to Wu et al.</u>

Claims 13 through 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hang (U.S. Patent No. 5,487,049) in view of Wu et al. (U.S. Patent No. 6,329,997). Applicant

respectfully traverses this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
>
> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 13-16 are improper because the elements for a prima facie case of obviousness are not met. Specifically, the rejection fails to meet the criterion that the prior art reference must each or suggest all the claim limitations.

Regarding independent claim 13 and claims 14-16 depending therefrom, Hang and Wu, the Office Action states:

> As per claims 13 and 16, Hang teaches the invention as set forth above for claim 1. However, Hang does not teach that the system is embodied on a semiconductor substrate (semiconductor wafer). Wu et al. teaches that is was known to incorporate a FIFO on the same substrate with a DRAM. See column 3, lines 8-20. It would have been obvious to one of ordinary skill in the art to have incorporated a FIFO with a DRAM on a single semiconductor substrate/wafer, as suggested by Wu et al., ... (Office Action p. 12).

Regarding the Office Action's characterization of Hang's teachings "as set forth above for claim 1", the Office Action states:

> As per claim 1, Hang teaches, with respect to figure 1, a DRAM 16, a DRAM controller for controlling the DRAM (see column 4, line 30), and a FIFO 10 associated with the DRAM (see column 2, lines 60-63). Hang further teaches at column 3, lines 63-67, that the data register 30 is a two-port memory which can simultaneously write data to a storage location having an address specified by a write count value while reading data from a different storage location having an address specified by a read count value. The claimed "control logic" is represented, at the least, by write counter 22, read counter 26, and state machine 20, as shown in figure 1. The FIFO temporarily stores addresses until a full page worth of data is stored in the data register for transfer to the DRAM. (Office Action p. 7).

Regarding claim 13, Hang teaches or suggests a page mode-directed FIFO, as herein described by the Office Action. Specifically, the Hang reference teaches or suggests:

> a FIFO interface between a system bus and a DRAM that transfers data to the DRAM utilizing the high speed page mode [wherein] words transferred having the same row address are accumulated in a store and then transferred to the DRAM utilizing the page mode to reduce the transfer time.
>
> According to another aspect of the invention, the words stored in FIFO are transferred to the DRAM when the row address of a next word to be stored changes so that the page mode transfer can be utilized. (Col. 1, lines 39-48).

In essence, the Hang reference teaches or suggests using a FIFO in conjunction with a memory device for buffering ***data that is to be transferred to memory once the command configures the control circuitry in a page mode configuration.*** Generally, Hang allows the memory command to ***configure the memory*** (in contrast to the memory command being stored in the FIFO) to operate in page mode and then ***buffer-up*** or burst-out ***memory data*** rather than buffering memory commands as claimed by the Applicants. In contrast and generally opposite, Applicants' inventions as respectively claimed in independent claim 13 is drawn to:

> 13. A semiconductor substrate including a DRAM, comprising:
> at least one memory bank;
> control logic associated with the at least one memory bank to control at least one of data and commands within the DRAM; and
> a FIFO associated with the control logic, the ***FIFO configured for temporarily storing a memory command until data corresponding to the memory command arrives at the DRAM***, the control logic further configured for simultaneous reading and writing of the at least one of data and commands from the FIFO. (Emphasis added.)

As stated, the Office Action cited Wu for it teachings relating to "incorporate[ing] a FIFO on the same substrate with a DRAM" which does not augment the teachings of Hang in such a manner as to render obvious Applicants' invention as claimed. Therefore, Applicants respectfully request the rejection of claim 13 and claims 14-16 depending therefrom be withdrawn.

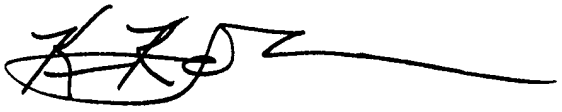
ENTRY OF AMENDMENTS

The amendments to claims 1, 6, 8, 17, 21 and 23 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search.

CONCLUSION

Claims 1 through 25 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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